a global video bus which routes the video data between said processing module and said at least one video processing module; and

a global control bus which provides said control data to/from said processing module from/to said at least one video processing module, said global control bus being separate from said [video data on said] global video bus.

2. (Amended) The system of claim 1, wherein said video data is coupled with associated video timing signals [information] synchronized to a system clock signal, and each video processing module comprises a crosspoint switch which routes said video data and its associated video timing signals [information] to/from respective ones of the parallel pipelined video hardware components, said timing [data] signals indicating when the video data represents active video information [compensating for pipeline delay in said video processing module].

Cl Cont.

3. (Amended) The system of claim 2, wherein each video processing module further comprises a crosspoint switch state machine which monitors transfers of video data over each data path of said crosspoint switch and facilitates [selection of idle data] allocating paths for [each transfer of data from one] transferring the video data among the parallel pipelined video hardware [component to another] components.

Sub B2

4. (Amended) The system of claim 2, wherein at least one video processing module comprises a configurable arithmetic logic unit (CALU) responsive to said video data and its associated video timing [information] signals so as to automatically compensate for differences in input video timing between respective images and to provide dual image pointwise video processing operations and image accumulations.

5. (Amended) The system of claim 2, wherein at least one video processing module comprises at least one pyramid filtering processor which generates [pyramid] spatially filtered representations of the video data at respectively different resolutions so as to facilitate real-time processing of said

video data [for said particular image processing tasks of said video processing system].

6. (Amended) The system of claim 2, wherein the modular video processing system includes a plurality of video processing modules and each video processing module comprises a connection for at least one daughterboard [which performs a video processing function on said video data which is unique to particular image processing tasks of said video processing system] the connection including means for routing at least a portion of the control data between the processing module and the daughterboard and for coupling the daughterboard to the ~~crosspoint switch.~~

16 7. (Amended) The system of claim 6, [wherein said at least one] further including a daughterboard [comprises] comprising a display processor card coupled to the daughterboard connection of one of the plurality of video processing modules, the display processor card including video input [and output] ports connected to said crosspoint switch and an encoder which converts video data received at [an] at least one of the input [port] ports into a video signal of a predetermined format for display.

17 8. (Amended) The system of claim 6, [wherein said at least one] further including a daughterboard [comprises] comprising a digitizer card coupled to the daughterboard connection of one of the plurality of video processing modules, the digitizer card including video [input and] output ports connected to said crosspoint switch and a decoder which decodes and digitizes video data received at [an] at least one input port into a video signal of a predetermined format [for further processing so as to provide an input and output interface for digital video] and provides the digitized video data to at least one of the output ports.

18 9. (Amended) The system of claim 6, [wherein said at least one] further including a daughterboard [comprises] comprising a correlator card coupled to the daughterboard connection of one of the plurality of video processing

modules, the correlator card including a plurality of video input and output ports connected to said crosspoint switch and a plurality of video processing channels, each channel comprising a configurable arithmetic logic unit, a pyramid filtering processor, and a look up table [which correlate respective images in each video processing channel in a predetermined manner].

19 17
~~10~~. (Amended) The system of claim ~~6~~, [wherein said at least one] further including a daughterboard [comprises] comprising a warper card coupled to the daughterboard connection of one of the plurality of video processing modules, the warper card including video input and output ports connected to said crosspoint switch, [and an address generator and] a pair of memory banks, an address generator, for controlling memory read operations and memory write operations in the memory banks, and a bilinear interpolator [for parametric transformation of video data received at an input port].

A1 Cont.

20 19
~~11~~. (Amended) The system of claim [6] ~~10~~, wherein said [at least one daughterboard comprises a warper card including a plurality of video input and output ports connected to said crosspoint switch, a pair of memory banks, and a plurality of] address generator and said bilinear interpolator are implemented as at least one field programmable gate array [arrays programmed so as to provide parametric transformation of video data received at said input ports].

Sub C2

12. (Amended) The system of claim 1, wherein said processing module comprises at least two microprocessors each of which has an associated random access memory which is not shared with any other microprocessor, [and] said processing module further comprising a shared memory which is accessible by each microprocessor of said processor module through an arbitrated control bus which arbitrates requests for access to said shared memory from each microprocessor.

Sub B4

13. (Amended) The system of claim 12, wherein said processing module includes means for using the control data to program the at least one video

processing module to perform at least one of the different video processing operations on the video data and means for providing a [provides at least one] synchronous start signal to begin the at least one video processing operation [for each different video processing operation of each video processing module].

5 ~~14.~~ (Amended) The system of claim 3 ~~12~~, wherein said processing module further comprises a communications [devices] interface for communicating with external devices, said communications [devices] interface being [accessed by each of said microprocessors via] coupled to said arbitrated control bus for access by each of said at least two microprocessors.

6 ~~15.~~ (Amended) The system of claim 3 ~~12~~, wherein said random access memory associated with each microprocessor is connected to said global video bus [and stores] to store video data for transmission to, and [stores] video data received from [said at least one video processing module over] said global video bus.

a' Cont.

7 ~~16.~~ (Amended) The system of claim 3 ~~12~~, wherein said processor module further comprises a semaphore register [available to each microprocessor via] coupled to said arbitrated control bus, said semaphore register storing semaphores so as to facilitate coordination of [and mutual exclusion of] mutually exclusive operations by said at least two microprocessors.

Sub C3

~~17.~~ (Amended) The system of claim 1, further comprising a hardware control library loaded on a general purpose microprocessor of said processing module, said hardware control library comprising a set of functions for programming the parallel pipelined video hardware of said at least one video processing module to perform [predetermined] respective ones of said different video processing operations concurrently.

9 ~~18.~~ (Amended) The system of claim 8 ~~17~~, wherein said processing module comprises at least two general purpose microprocessors and said hardware control library further comprises a set of functions for coordinating concurrent

multitask processing operations of said at least two general purpose microprocessors.

19. (Amended) The system of claim 17, wherein said control data comprises [video device information] respective control signals for each hardware component of said video processing system, wherein said functions of said hardware control library manipulate said [video device information] control signals to program said hardware components for each of said different video processing operations.

20. (Amended) A method of creating a modular video processing system, comprising the steps of:

providing video data via a global video bus;

providing a global control bus;

connecting [to a global control bus] a processing module containing at least one general purpose microprocessor to said global video bus and said global control bus [which controls] said microprocessor controlling hardware and software [operation] operations of said video processing system using control data and processing said video data;

connecting to said global control bus and said global video bus to at least one video processing module which contains parallel pipelined video hardware [which is programmable by] that is responsive to said control data to provide different video processing operations on [an input stream of] the video data;

wherein said processing module [detecting] detects the presence of each video processing module connected to said global control bus; and [said processing module passing] passes said control data to each detected video processing module over said global control bus to program said parallel pipelined video hardware to perform [a video processing function which is unique to particular processing tasks of said video processing system] at least one of said video processing operations.

21. (Amended) The method of claim 20, comprising the additional steps of [coupling to a global video bus said video data with] connecting the hardware components of the processing module to a crosspoint switch and providing associated video timing [information] signals with the video data, said video timing signals being synchronized to a system clock signal, and routing said video data and [its] associated video timing [information] signals to/from respective parallel pipelined video hardware components of said video processing module over said global video bus via [a] the crosspoint switch, said timing signals indicating when the video data represents active video information [data compensating for pipeline delay in said video processing module].

22. (Amended) The method of claim 21, comprising the additional step of [said processing module] providing at least one synchronous start signal [to each detected video processing module over] via said global control bus said synchronous start signal being coupled to the processing module and to the at least one video processing module to signal the start of the at least one video processing operation.

23. (Amended) The method of claim 22, comprising the additional step of coupling a semaphore register to the processing module said semaphore register being configured to coordinate [coordinating] multitask processing operations when said processing module comprises at least two general purpose microprocessors.

24. (Amended) The method of claim 21, comprising the additional steps of connecting a crosspoint state machine to said crosspoint switch, said crosspoint state machine monitoring transfers of video data over each data path of said crosspoint switch and [facilitating selection of idle data] allocating paths for [each transfer of data from one] transferring the video data among the parallel pipelined video hardware [component to another] components.

25. (Amended) The method of claim 21, wherein said control data comprises [video device information] respective control signals for each hardware component of said video processing system, [comprising the further step of said] the method including the step of coupling said processing module [manipulating] to manipulate said [video device information] control signals to program said hardware components for each of said different video processing operations.

26. (Amended) The method of claim [21] 22, comprising the steps of configuring the video processing module to automatically [compensating] compensate for differences in input video timing between respective [images] combinations of video data and video timing signals provided by said crosspoint switch and [providing] to provide dual image pointwise video processing operations and image accumulations of said respective images.

27. (Amended) A modular processing system comprising:

at least one specialized processing module which contains parallel pipelined hardware [which] that is programmable to provide different specialized processing operations on an input stream of data;

a general processing module containing a general purpose microprocessor which controls hardware and software operation of said specialized processing module and said general processing module, using a hardware control library loaded on said general purpose microprocessor, said hardware control library comprising a set of functions for programming said parallel pipelined hardware of said at least one specialized processing module and said microprocessor of said general processing module to perform predetermined specialized processing operations on the input stream of data; and

a global control bus which provides control data to/from said hardware control library of said general processing module from/to said at least one specialized processing module separate from said stream of input data to be